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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,644	05/19/2004	Mark D. Dupuis	BUR920040106US1	3643

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ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/709,644	Mark D. Dupuis
	Examiner	Art Unit
	Trung Dang	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 2/21/05

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453.O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-35 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 28-32 is/are allowed.

6)☒ Claim(s) 1,8-14,21 and 33-35 is/are rejected.

7)☒ Claim(s) 2-7,15-20 and 22-27 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 8-11 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Coolbaugh et al. (US 2002/0185708).

The rejection is maintained as of record and is repeated herein.

With reference to Figs. 2-4, the reference teaches the claimed invention in that it discloses a method for forming semiconductor structures, the method comprising the steps of:

(a) forming a first plurality of identical semiconductor structures, wherein each of the first plurality of identical semiconductor structures is formed by:

(i) forming a first region **16** of single crystal Si and a second region **12** of insulating material, wherein the first region and the second region are in direct

physical contact with each other via a first common interface surface (Fig.2) , and

(ii) depositing SiGe simultaneously on top of the first and second regions so as to grow third region **26** of single crystal SiGe and fourth region **24** of polycrystalline SiGe from the first and second regions, respectively, such that a second common interface surface between the third and fourth region grows from the first common interface surface, wherein the first and third regions comprise a same material and have single-crystal atoms arrangement, wherein the first region has a different atoms arrangement than the fourth region, and wherein the step of depositing the growth material is performed under a first deposition condition (Fig. 4 and related text).

Note that independent claims 1 and 14 recite an "if" condition, which include an option where the first yield of the first plurality of identical semiconductor structures is within a pre-specified range, leading to a second run to form a second plurality of identical semiconductor structures being not carried out. In this instant, the reference reads on every limitation of the claims.

As for newly added claims 33 and 34, the condition of which whether or not step (b) is carried out is independent from the definition of the first yield. Namely, no matter what the first yield is defined, the "if" condition recited in the claims always

implies the option as noted above, hence the reference still reads on the claimed limitation.

3. Claim 21 is rejected under 35 U.S.C. 102(b) as being anticipated by Emons et al. (US 6,100,152).

The rejection is maintained as of record and is repeated herein.

With reference to Figs. 1-3, Emons teaches a method for forming semiconductor structures, the method comprising the steps of:

(a) forming a first plurality of identical semiconductor structures, wherein each of the first plurality of identical semiconductor structures is formed by:

(i) providing a silicon substrate (col. 3, lines 65-67);

(ii) forming a single-crystal silicon layer **3** on the substrate;

(iii) forming first and second shallow trench isolation regions **8** in the single-crystal silicon region **3**, the first and second shallow trench isolation regions defining a first single-crystal silicon region **3** sandwiched between the first and second shallow trench isolation regions;

(iv) growing a seed layer **4** of polysilicon on top of the first and second shallow trench isolation regions **8** (Fig. 1);

(v) depositing silicon and germanium simultaneously (A) on top of the first single-crystal silicon region **3** so as to grow a second single-crystal silicon region **1A** and (B) on top of the first and second shallow trench isolation regions **8** so as to grow first and second polysilicon regions **1B**, respectively, wherein the

second single-crystal silicon region **1A** and the first polysilicon region **1B** are in direct physical contact with each other, wherein the second single-crystal silicon region **1A** and the second polysilicon region **1B** are in direct physical contact with each other (Fig.3 and related text); and

wherein the step of depositing silicon and germanium is performed under a first deposition condition (paragraph bridging col. 4 and col. 5).

Note that the claim recites an "if" condition, which includes an option where the first yield of the first plurality of identical semiconductor structures is within a pre-specified range, and a second run to form a second plurality of identical semiconductor structures is not carried out. In this instant, the reference reads on every limitation of the claims.

As for the newly added claim 35, the condition of which whether or not step (b) is carried out is independent from the definition of the first yield. Namely, no matter what the first yield is defined, the "if" condition recited in the claims always implies the option as noted above, hence the reference still reads on the claimed limitation

4. Claims 1, 12 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Khater et al. (US 2004/0188797).

The rejection is maintained as of record and is repeated herein.

With reference to Figs. 2E- 2H, Khater teaches a method for forming semiconductor structures, the method comprising the steps of:

(a) forming a first plurality of identical semiconductor structures, wherein each of the first plurality of identical semiconductor structures is formed by:

(i) forming a first region **AA** of single crystal Si and a second region **STI** of insulating material, wherein the first region and the second region are in direct physical contact with each other via a first common interface surface;

(ii) forming a seed layer **UP1** on top of the first region **AA** and the second region **STI** (Fig. 2E);

(iii) removing a portion of the seed layer on top of the first region **AA** (Fig. 2G);

(iv) depositing SiGe simultaneously on top of the first and second regions so as to grow third region **IB** of single crystal SiGe and fourth region **DP1** of polycrystalline SiGe from the first and second regions, respectively, such that a second common interface surface between the third and fourth region grows from the first common interface surface, wherein the first and third regions comprise a same material and have single-crystal atoms arrangement, wherein the first region has a different atoms arrangement than the fourth region, and wherein the step of depositing the growth material is performed under a first deposition condition (Fig. 2H and related text).

Note that independent claim 1 recites an "if" condition, which include an

option where the first yield of the first plurality of identical semiconductor structures is within a pre-specified range, and a second run to form a second plurality of identical semiconductor structures is not carried out. In this instant, the reference reads on every limitation of the claims.

Allowable Subject Matter

5. Claims 2-7, 15-20, 22-27, ~~and 30~~ are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Note the statement of reasons for the indication of allowable subject matter in previous office action.

6. Amended claims 28-32 are allowed over prior art of record.

7. The following is an examiner's statement of reasons for allowance:

Amended claims 28-32 are allowed because prior art of record does not teach or suggest the claimed limitation regarding the yield of the semiconductor structure design is a function of a percentage of satisfaction structures of a plurality of semiconductor structures formed according to the semiconductor structure design in all the plurality of semiconductor structures.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

8. Applicant's arguments filed 2/21/05 have been fully considered but they are not persuasive..

With respect to Coolbaugh et al. reference applicants argue that Coolbaugh does not teach step (b) as recited in claim 1. The Examiner agrees that Coolbaugh does not teach step (b). However, as noted in the rejection, step (b) of claim 1 is not necessarily always carried out because of the "if" condition. Particularly, step (b) implies two alternatives:

1) If a first yield is not satisfied then forming a second plurality of identical semiconductor structure.

2) If a first yield is satisfied then the step of forming a second plurality of identical semiconductor structure is not necessarily.

In examining an application for patent, it is well settle that the claims have to be read in light of the specification in order to determine the scope of the invention. In this respect, paragraphs [0027]-[0028] of the specification clearly indicates such alternatives. In the case of 2), Coolbaugh 's reference reads on the claimed limitation as noted in the rejection.

Applicants further argue that claim 1 does not explicitly or implicitly include such conditional step as alleged by the Examiner. The Examiner disagrees because the term "if" itself implies a condition on which something depends.

As for the rejection of claim 21 by Emons and the rejection of claims 1, 12, and 13 by Khater, similar for the response with respect to claim 1 above, the Examiner's position is that the applied references read on the claimed limitation as noted in the rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang

Trung Dang
Primary Examiner
AU 2823

5/02/05